REMARKS

Claims 1-7 and 9 have been examined and claim 8 is withdrawn from consideration. Claims 1-7 and 9 are amended herein and are now pending in the application. It is noted with appreciation that claims 6 and 7 are deemed to be directed toward allowable subject matter. A proposed drawing correction attached hereto. Reexamination and reconsideration of all outstanding objection and rejections is requested.

Claims 1-7 and 9 are rejected under 35 U.S.C. §112, second paragraph as being indefinite. All the examiners comments have been carefully considered and the claims have been amended in accordance with the comments and suggestions.

Claims 1-3 and 9 are rejected under 35 U.S.C. §102(b) as being anticipated by Dhong et al.

Claim 1, as currently amended, recites a tri-stable MOS latch having first and second series circuits, each including a MOS transistor and a biasing elements for biasing the MOS transistor, and also recites a feedback network coupling the first and second series circuits. The biasing elements create substantially identical voltage drops to bias the MOS transistors in triode mode so to a achieve a third stable operating point.

The Dhong reference discloses a improved sense amplifier. The sense amplifier is a latch and includes two series circuits and a feedback circuit. As described in column 4, lines 32-38 and column 5, lines 16-20 of Dhong, the function of the series p-channel transistors is to clamp the bit lines to a minimum voltage higher than 0 and the transistors are biased to achieve this clamping. The nodes of the sense amplifier retain a full VDD swing. Col. 5, line 43. As is well known in the art, to achieve a full voltage swing requires one transistor to biased ON and the other to be biased off to achieve two stable operating points.

The examiner states that the Dhong reference discloses the topology recited in claim 1 and that the limitation of biasing the MOS transistors in triode mode to achieve a third operating point is also met because the structure of the claim is fully met.

This rejection is respectfully traversed for the following reasons. As described above and stated by the examiner, there is no disclosure of the functional limitation that the bias elements create substantially identical voltage drops to bias the MOS transistors in triode mode to achieve a

third stable operating point. It is respectfully asserted that this limitation is not fully met by the mere recitation of a similar topology in Dhong.

The inventors have discovered that the latch recited in the claim will achieve a third stable operating point when the MOS transistors are biased in triode. There is no disclosure of this property in Dhong or any other cited reference.

In Dhong the latching transistors are biased to clamp the downward voltage swing of the bit lines to a clamped voltage. As described in the Abstract, one node of the sense amplifier retains a full VDD swing as is connected to the DATA line.

As determined by the CAFC, functional limitations may be utilized if the functional limitation is described in the specification and is not indefinite. In the present application the biasing elements are disclosed in detail in Figs. 11 and 12. Further, the biasing of MOS transistors in triode mode is understood by persons of skill in the art and can be implemented utilizing the present specification as a guideline.

Accordingly, there is no disclosure or suggestion in Dhong of the claimed combination and claim 1 in not anticipated by Dhong.

Claim 9 recites a method for utilizing an MOS circuit, biased to cause the MOS circuit to have 3 stable operating points, including the steps of coupling a ternary logic signal to the MOS circuit, latching the state of the ternary logic signal, and utilizing the state latched to perform ternary logic functions.

The examiner states the Fig. 9 of Dhong discloses a circuit as recited in claims 1-3 and it is seen that operating a latch in a ternary logic unit is the intended use (i.e., it is up to the designer to use the latch circuit in any environment such as in a memory unit or in a ternary unit depending on the application).

This rejection is respectfully traversed for the following reasons. As described above, Dhong describes a latch used in a sense amplifier that retains the full swing of VDD, i.e., either VDD or 0. Accordingly, the latch of Dhong would be useless to a designer implementing a ternary unit.

The inventors are the first to design an MOS latch circuit that has 3 stable operating points to enable latching the states of a ternary signal for use in a ternary logic circuit. There is no disclosure in Dhong of a MOS circuit that can be utilized in a ternary logic and, thus, claim 9 is not anticipated by that reference.

Claims 1, 2, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heightley et al. in view of Wrathall et al.

The invention, as defined by claims 1 and 9 is described above.

The reference Heightley discloses a diode-coupled semiconductive memory that uses a flip-flop (Fig. 2) as a storage device. Col. 4, line 17. As described at col. 4, line 37, the flip-flop is either "on" or "off" and has two stable operating points. These two stable operating points are achieved by having one transistor biased in the ON state and the other in the OFF state. Col. 3, line 36.

The examiner states that the Heightley reference discloses the topology recited in claim 1, except for implementation in MOSFET technology, and that the limitation of biasing the MOS transistors in triode mode to achieve a third operating point is also met because the structure of the claim is fully met. Wrathall is cited to show that utilizing MOSFET technology is obvious.

This rejection is respectfully traversed for the following reasons. As described above and stated by the examiner there is no disclosure of the functional limitation that the bias elements create substantially identical voltage drops to bias the MOS transistors in triode mode to achieve a third stable operating point. However, it is respectfully asserted that this limitation is not fully met by the mere recitation of a similar topology in Heightley.

The inventors have discovered that the latch recited in the claim will achieve a third stable operating point when the MOS transistors are biased in triode. There is no disclosure of this property in Heightley or any other cited reference.

In Heightley one of the transistors is biased ON and the other OFF to achieve two stable operating states.

As determined by the CAFC, functional limitations may be utilized if the functional limitation is described in the specification and is not indefinite. In the present application the biasing elements are disclosed in detail in Figs. 11 and 12. Further, the biasing of MOS transistors in triode mode is understood by persons of skill in the art and can be implemented utilizing the present specification as a guideline.

Accordingly, there is no disclosure or suggestion in Heightley singly or in combination with Wrathall of the claimed combination .

Claim 9 recites a method for utilizing an MOS circuit, biased to cause the MOS circuit to have 3 stable operating points, including the steps of coupling a ternary logic signal to the

MOS circuit, latching the state of the ternary logic signal, and utilizing the state latched to perform ternary logic functions.

The examiner states the combination of Heightley and Wrathall discloses a circuit as recited in claims 1-3 and it is seen that operating a latch in a ternary logic unit is the intended use (i.e., it is up to the designer to use the latch circuit in any environment such as in a memory unit or in a ternary unit depending on the application).

This rejection is respectfully traversed for the following reasons. As described above, Heightley describes a latch used in a sense amplifier that retains the full swing of VDD, i.e., either VDD or 0. Accordingly, the latch of Heightley would be useless to a designer implementing a ternary unit.

The inventors are the first to design an MOS latch circuit that has 3 stable operating points to enable latching the states of a ternary signal for use in a ternary logic circuit. There is no disclosure in Heightley singly or in combination with Wrathall of a MOS circuit that can be utilized in a ternary logic and, thus, claim 9 is not anticipated by that reference.

Claims 1, 3, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Waaben in view Wrathall.

The invention defined by claim 1 is described above.

Waaben discloses a low-power flip-flop circuit. As described at col. 2, line 55 only of the two transistors is conducts during steady state operation, the other is off. Thus, two stable states exist.

The examiner states that the Waaben reference discloses the topology recited in claim 1, except for implementation in MOSFET technology, and that the limitation of biasing the MOS transistors in triode mode to achieve a third operating point is also met because the structure of the claim is fully met. Wrathall is cited to show that utilizing MOSFET technology is obvious.

This rejection is respectfully traversed for the following reasons. As described above and stated by the examiner there is no disclosure of the functional limitation that the bias elements create substantially identical voltage drops to bias the MOS transistors in triode mode to achieve a third stable operating point. However, it is respectfully asserted that this limitation is not fully met by the mere recitation of a similar topology in Waaben.

The inventors have discovered that the latch recited in the claim will achieve a third stable operating point when the MOS transistors are biased in triode. There is no disclosure of this property in Heightley or any other cited reference.

In Waaben one of the transistors is biased ON and the other OFF to achieve two stable operating states.

As determined by the CAFC, functional limitations may be utilized if the functional limitation is described in the specification and is not indefinite. In the present application the biasing elements are disclosed in detail in Figs. 11 and 12. Further, the biasing of MOS transistors in triode mode is understood by persons of skill in the art and can be implemented utilizing the present specification as a guideline.

Accordingly, there is no disclosure or suggestion in Heightley singly or in combination with Wrathall of the claimed combination .

Claim 9 recites a method for utilizing an MOS circuit, biased to cause the MOS circuit to have 3 stable operating points, including the steps of coupling a ternary logic signal to the MOS circuit, latching the state of the ternary logic signal, and utilizing the state latched to perform ternary logic functions.

The examiner states the combination of Waaben and Wrathall discloses a circuit as recited in claims 1 and it is seen that operating a latch in a ternary logic unit is the intended use (i.e., it is up to the designer to use the latch circuit in any environment such as in a memory unit or in a ternary unit depending on the application).

This rejection is respectfully traversed for the following reasons. As described above, Waaben describes a latch used in a sense amplifier that retains the full swing of VDD, i.e., either VDD or 0. Accordingly, the latch of Waaben would be useless to a designer implementing a ternary unit.

The inventors are the first to design an MOS latch circuit that has 3 stable operating points to enable latching the states of a ternary signal for use in a ternary logic circuit. There is no disclosure in Waaben singly or in combination with Wrathall of a MOS circuit that can be utilized in a ternary logic and, thus, claim 9 is not anticipated by that reference.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Heightley in view of Wrathall and further in view of Arcus.

Claim 4 is similar in scope to claim 1 and is implemented in CMOS technology.

The disclosure of Heightley and Wrathall is described above.

Arcus discloses a charge pump implemented in CMOS technology.

The examiner states that the Heightley reference discloses the topology recited in claim 1, except for implementation in MOSFET technology, and that the limitation of biasing the MOS transistors in triode mode to achieve a third operating point is also met because the structure of the claim is fully met. Wrathall is cited to show that utilizing MOSFET technology is obvious. Arcus is cited to show using a PMOS transistor as a loading element.

This rejection is respectfully traversed for the following reasons. As described above and stated by the examiner there is no disclosure of the functional limitation that the bias elements create substantially identical voltage drops to bias the MOS transistors in triode mode to achieve a third stable operating point. However, it is respectfully asserted that this limitation is not fully met by the mere recitation of a similar topology in Heightley.

The inventors have discovered that the latch recited in the claim will achieve a third stable operating point when the MOS transistors are biased in triode. There is no disclosure of this property in Heightley or any other cited reference.

In Heightley one of the transistors is biased ON and the other OFF to achieve two stable operating states.

As determined by the CAFC, functional limitations may be utilized if the functional limitation is described in the specification and is not indefinite. In the present application the biasing elements are disclosed in detail in Figs. 11 and 12. Further, the biasing of MOS transistors in triode mode is understood by persons of skill in the art and can be implemented utilizing the present specification as a guideline.

Accordingly, there is no disclosure or suggestion in Heightley singly or in combination with Wrathall and/or Arcus of the claimed combination .

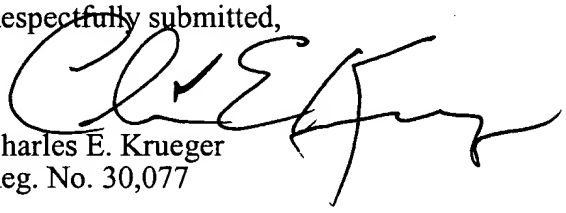
Claim 5 depends on claim 4 and is patentable for the same reasons as claim 4.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this Application are in condition for allowance. The issuance of a formal Notice of Allowance at an early date is respectfully requested.

If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at (925) 944-3320.

Respectfully submitted,



Charles E. Krueger
Reg. No. 30,077

LAW OFFICE OF CHARLES E. KRUEGER
P.O.Box 5607
Walnut Creek, CA 94596
Tel: (925) 944-3320 / Fax: (925) 944-3363